GOSSIPO-3: Measurements on the Prototype of a Read-Out Pixel Chip for Micro-Pattern Gas Detectors

André Kruth¹, Christoph Brezina¹, Sinan Celik², Vladimir Gromov², Ruud Kluit², Francesco Zapon², Klaus Desch¹, Harry van der Graaf²

¹Physics Department, University of Bonn, Nussallee 12, 53115 Bonn, Germany
²National Institute for Subatomic Physics (Nikhef), Science Park 105, 1098 XG Amsterdam, The Netherlands

TWEPP, Aachen September 20th-24th 2010
Outline

• Read-Out of Ingrid-Gaseous Detectors
• GOSSIPO-3: Features & Architecture
• Measurement Results & Discussion
• Summary & Outlook
Read-Out of Ingrid-Gaseous Detectors

Gas-avalanche detector combining a gas layer as signal generator with a CMOS readout pixel array

- Particle track image (projection) with 3D track reconstruction
- No sensor leakage current compensation
- Low parasitic capacitance (less than 10fF)
- Single-electron efficiency by high gas gain
- Micro-discharges in avalanche gap
- Time (z-) resolution set by longitudinal diffusion
GOSSIPO-3 Features

• Small prototype for a read-out chip for MPGDs
• IBM 130nm CMOS (8 metal layers)
• 60µm x 60µm pixels (high granularity)
• ToA Measurement and ToT Measurement [Charge]
• Local TDC in every pixel
• Design Goals:
  – 3µW per channel
  – Arrival time measurement up to 102µs
  – Arrival time accuracy 1.6ns (one fast VCO bin)
  – ToT accuracy 200e- accuracy (<50ns)
Pixel Electronics

- Pad → Preamp → Discr. → HIT
- Threshold Mask
- Threshold DAC
- Local Fast Oscillator 640 MHz
- 4 Bit Fast ToA Counter
- 12 Bit Slow ToA Counter
- 8 Bit Slow ToT Counter
- LFSR = Counters (data taking) or Shift Registers (data read-out)

Control Signals:
- Common Stop
- Reset
- Clock
- Token

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Common-Stop Timing Scheme

- Fast clock: 640MHz (1.6ns time bins), started by discriminator
- Slow clock: 40MHz (25ns time bins), absolute external timing
GOSSIPO-3 Architecture

- 3 Front-Ends (preamp, comp)
- Pixel (pre-amplifier, comp, Threshold DAC, high resolution TDC (VCO), counters & control logic)
- 2 LDOs (generate controllable Power Supply Voltage of Ring Oscillators)

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Demonstrator Test Set-Up

- Power Regulators
- Demonstrator
- SRAM
- USB Port
- FPGA
- μC
- External Bias
- Overwrite
- G3 Test Board (dedicated PCB)
- S3 Multi IO Board (general purpose test board designed by Bonn group)

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Front-End Performance

- Pre-Amplifier with MOSFET feedback parasitic capacitance
- $C_{FB}$ about 1fF – high gain
- Low parasitic input capacitance

\[ C_{FB} = C_{DS} + C_{DG} + C_{DB} + C_{DJ} \approx 1 \text{ fF} \]

\[ C_{PAR} = 10 \text{ fF} \]

\[ I_{BIAS} = 6 \text{ nA} \]

\[ C_{AC} = 170 \text{ fF} \]
Front-End Performance

- Excellent pre-amplifier noise performance
  - Charge injection through test pad
  - Measurement includes output pad driver
  - Measured and simulated
    \[ \sigma_{\text{NOISE}} \sim 4 \text{mV} \Rightarrow \text{ENC} \sim 25 \text{e}^- \]

\[\Delta V = 64 \text{mV}\]

\[V_{\text{PK-PK}} < 20 \text{mV}\]
Front-End Performance

- Pre-amplifier measurement for different channels
  - Metal-Metal Injection Capacitance $C_{TEST} \sim 1 \text{fF}$
  - Stable high gain
  - Varying time constant of feedback discharge

$U_{IN} \cdot C_{TEST1}/C_{FB1}$

$U_{IN} \cdot C_{TEST2}/C_{FB2}$

$U_{IN} \cdot C_{TEST3}/C_{FB3}$

$C_{TEST}$ and $C_{FB}$ are well reproducible
• **ToT measurement for different channels**
  
  - \( Q_{\text{IN}} = 375e^- \)
  
  - ToT channel to channel mismatch up to 50% w/o offline calibration
  
  - Jitter on TOT trailing edge caused by noise on pre-amplifier signal trailing edge
  
  - Cross-talk between channels observed when pad driver switches
Front-End Performance

- Analysis of time variation of the feedback discharge
  - Process variation of small feedback MOSFET responsible for variation of feedback current
  - Small feedback MOS needed for high gain

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Front-End Performance

- Internal delay [including pad drivers] due to time walk
  - 6ns asymptotical delay for a charge >6000e⁻
  - Delay injection to comparator >1.6ns TDC bin
  - Further reduction of delay saves offline calibration

![Delay injection to comparator graph]

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
LDO Performance

- LDO controls supply voltage of fast TDC ring-oscillator (arrival time measurement)
- Oscillation frequency of $f=640\text{MHz}$ in all process corners
  - Time bin size $T=1.56\text{ns}$
  - Maximum run time $25\text{ns}$ (16 bins)
  - $V_{\text{OUT}_{-LDO}}=0.61\text{V}$ (fast corner)..$1.10\text{V}$ (slow corner)
- Occupancy expectation gives
  - avg. $\Delta I_{\text{OUT}_{-LDO}}=24\text{mA}$
  - peak $\Delta I_{\text{OUT}_{-LDO}}=44\text{mA}$
- VCO control characteristic allows for max. $\Delta V_{\text{LDO\_OUT}}=31\text{mV}$ for $25\text{ns}$
LDO Performance

- Step response to typical load step of 20mA
  - Load externally connected
  - Inductance of package and bond wires limits response time

![Graph showing step response to load step with curves for small and large LDOs.](Image)
LDO Performance

- Settling time to nominal $V_{OUT}$ value for different (external) load steps

![Graph showing settling time for different load steps]

Settling Accuracy 2%
Settling Accuracy 4%

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
TDC Performance

- Counting steps of TDC (input signal directly at digital logic)

Digital Delay Scan, 200 Pulses each

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Pixel Performance

- Counting steps of TDC (input signal at analog input)

Complete Pixel Delay Scan @1V, 200 Pulses each

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Summary

- Successful operation and measurements:
  - Front-End:
    - Internal delay limited by pad drivers
    - Source of pixel to pixel TOT mismatch identified
    - High gain / low noise
  - LDOs:
    - Step response time critical for TDC performance
    - Close match between simulation and measurement
  - TDC:
    - Transition region of counting steps ~25% of TDC bin (wc)
    - Bin size / fast oscillator frequency reproducible for multiple channels and chips
- Gossipo-3 design team joins Timepix II design efforts
  - Timepix II will benefit from lessons learned
Thanks for your attention!
Backup Slides
Pre-Amplifier Schematic

$I_{BIAS} = 6 \text{ nA}$

$C_{FB} = C_{DS} + C_{DG} + C_{DB} + C_{DJ} \approx 1 \text{ fF}$

$C_{PAR} = 10 \text{ fF}$

$C_{AC} = 170 \text{ fF}$

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Pre-Amplifier Schematic

**Input stage**
- Vdd_ana
- 70 nA
- 720 nA
- 435 nA
- gm=23u
- Cpar ≈ 10 fF
- Preamp_in
- sub_preamp (0.2V)
- Uout_preamp

**Voltage follower**
- C*= 6f
- ncap
  - C=170fF
- Ron = 30MΩ
- Ron = 100MΩ

**Feedback**
- 6 nA
- 0.48/2.4
- 2.4/2.4
- 2nA
- 0.48/2.4
- 2.4/2.4

**Baseline recovery**
Front-End Performance

- Internal delay (very first measurements)
- 9ns asymptotical delay for a charge >6000e⁻ (injection to comparator) > 1.6ns TDC bin
- Further reduction of delay needed
Front-End Performance

- Simulated internal delay [Injection to Comparator Output] based on parasitic extraction
LDO Performance

- Static $R_{OUT}$ measurement

![Graph showing output impedance vs. current drawn for Small and Large LDO, with measurement and simulation data.](image)
LDO Performance

- Linearity measurement

![Graph showing output voltage vs. reference voltage for Small LDO and Large LDO]
LDO Performance

- Step response to maximum load step 40mA
  - additional external load
  - inductance of package and bond wires limit response time

![Graph showing step response to maximum load step 40mA for Small LDO and Large LDO.](image)
GOSSIP vs. TPC

- **GOSSIP**
  - Small drift gap (1mm)
  - Track perpendicular to read-out plane

- **TPC**
  - Large drift gap (1m)
  - Track parallel to read-out plane
Pixel Electronics

Block diagram of the pixel

- Preamp
- Discr.
- HIT
- Threshold - Mask
- Time / Counting
- 6 bit Pixel Configuration Memory
- Control
- Local fast VCO (640MHz)
- 4 bit Fast counter
- 8 bit ToT counter
- 12 bit Slow counter
- Threshold DAC

Control signals
- Clock
- TRIGGER (common stop)
- TOKEN
- RESET

LFSR = Counters (data taking)
or
LFSR = Shift registers (data read-out)

Layout of the pixel

Logic: Counters & Control

Oscillator

Preamp & Comparator

A. Kruth, GOSSIPO-3, TWEPP, Aachen, Sept. 20th-24th 2010
Outlook

- Larger pixel array needed for InGrid test
- The Gossipo-3 design team joins Timepix II design efforts